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EXAMINER	
UNELUS, ERNEST	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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DETAILED ACTION

RESPONSE TO AMENDMENT

Claim rejections based on prior art

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/19/08 has been entered.

Applicant's arguments filed 12/19/2008 with respect to claims 1-4, 6, 7, 10-22, 24-27, 29, 30, 32-53, 78-87, 90-93, and 97-103 have been fully considered but are moot in view of the new ground(s) of rejection.

The rejection(s) of claim(s) 1-4, 6, 7, 10-22, 24-27, 29, 30, 32-53, 78-87, and 89-95 over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) have been fully considered and is not persuasive. However, base on the amendment, the rejection has been withdrawn. Therefore, upon further consideration, a new ground(s) of rejection is made in view of Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and in further view of Rinaldis et al. (US pat. 7,107,343).

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

2. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-16, 20-37, 41-46, 50, 78-83, 86-87, 90-93, and 97-103**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and further in view of Rinaldis et al. (US pat. 7,107,343).

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5. As per **claims 1, 21, 78, and 90**, Bicknell discloses "A storage virtualization computer system **(system 100 of fig. 6)** comprising:

a host entity for issuing IO requests **(Host computer of fig. 6)**;

an external storage virtualization controller **(controller 1)** coupled to said host entity for executing IO operations in response to said IO requests **(see fig. 6 and paragraph 0029)**; and

a group of physical storage devices (PSDs) **(Discs in the disc pack 118 of disc drive 106, as discloses in paragraph 0018; see also figs. 3 and 6)**, each coupled to the storage virtualization controller through a point-to-point serial-signal interconnect **(see fig. 6 and paragraph 0019)**, for providing storage to the storage virtualization computer system through the storage virtualization controller **(see paragraph 0027)**,

wherein said computer system further comprises a detachable canister **(housing 116 of fig. 3, as discloses in para. 0018)** attached to said storage virtualization controller for containing one of said at least one PSDs therein **(see fig. 2 and see paragraph 0019, which discloses "Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100")**;

wherein said storage virtualization controller is configured to define at least one logical media unit **(disc pack 118 of fig. 3, as discloses in para. 0018)** consisting of sections of at least one said group of PSDs **(see fig. 2 and see paragraph 0024)**,

but fails to disclose expressly "wherein said storage virtualization controller comprises: a central processing circuitry for performing said IO operations in response to said IO requests of said host entity;

at least one IO device interconnect controller coupled to said central processing circuitry;

at least one host-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupling to said host entity; and

at least one device-side IO device interconnect port provided in one of said at least one IO device interconnect controller for coupled to said group of PSDs through said point-to-point

serial-signal interconnect, said device-side IO device interconnect port being a serial port for point-to-point serial-signal transmission; and

wherein said SVC issues a device-side IO request to said IO device interconnect controller, and said IO device interconnect controller re-formats said device-side IO request and accompanying I0 data into at least one data packet for transmission to said group of PSDs through said device-side IO device interconnect port".

Meehan discloses "wherein said storage virtualization controller comprises: a central processing circuitry **(microprocessor 406 of fig. 6, as discloses in para. 0028)** for performing said IO operations in response to said IO requests of said host entity **(see fig. 5 and para. 0028)**;

at least one IO device interconnect controller **(FPGA 409 of fig. 6, as discloses in para. 0028)** coupled to said central processing circuitry **(see fig. 6)**;

at least one host-side IO device interconnect port **("host interface 411 (from the host)", as discloses in para. 0029)** provided in one of said at least one IO device interconnect controller for coupling to said host entity **(see para. 0029, which discloses "Data to be written to storage disks 401-404 would move from the host interface 411 (from the host), optionally through a primary RAID Controller (if present), through the Interface connector 410, and into the buffer RAM 407 of RAID Controller 400")**; and

at least one device-side IO device interconnect port **("interface 411", as discloses in para. 0029)** provided in one of said at least one IO device interconnect controller for coupled to one of said at least one physical storage device through said point-to-point serial-signal interconnect **(see para. 0029 and fig. 6, which show the interface 411 as part of the controller; in other words, the drawing illustrated part of the interface 411 is inside the**

controller. See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal interconnect), said device-side IO device interconnect port being a serial port for point-to-point serial-signal transmission **(See para. 0029 and fig. 6 for SAS transmission and point-to-point serial-signal interconnect)**; and

wherein said SVC issues a device-side IO request to said IO device interconnect controller, and said IO device interconnect controller re-formats said device-side IO request and accompanying I0 data into at least one data packet for transmission to said PSD through said device-side IO device interconnect port" **(see para. 0029, which discloses the FPGA 409 'manipulating' data between the host and the storage devices. Manipulating is a form of 're-formatting'. The claim language is not specific as to how this reformatting is being done. See also para. 0016, which discloses 're-distributed' the data).**

Neither Bicknell nor Meehan discloses "wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual I0 information to transmit through the device-side I0 device interconnect, and a check data segment containing check codes derived from said payload data for checking the correctness of said payload data after transmission".

Rinaldis discloses "wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual I0 information to transmit through the device-side I0 device interconnect, and a check data segment containing check codes derived from said

payload data for checking the correctness of said payload data

after transmission" **(see col. 6, lines 20-25)**.

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), and Rinaldis et al. (US pat. 7,107,343) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, and a low cost system for providing improved RAID 1 performance as described Rinaldis.

The motivation for doing so would have been because Meehan teaches, "In addition, a RAID 0 stripe can be written to the storage devices at the same time. This stripe allows for the data to be evenly written to the devices 120 in an attempt to maximize overall system performance" (see paragraph 0006). See also col. 2, lines 44-46, which discloses "Accordingly, the present invention provides a RAID 1 controller that is capable of operating at higher speeds than conventional RAID 1 controllers".

Therefore, it would have been obvious to combine Rinaldis et al. (US pat. 7,107,343) and Meehan et al. (US pub. 2004/0177218) with Bicknell et al. (US pub. 2003/0193776) for the benefit of creating the computer system to obtain the invention as specified in claims 1, 21, 78, and 90.

6. As per **claims 2, 22, 79, and 91**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said point-to-point serial-signal interconnect is a Serial ATA IO device interconnect **(see fig.6 and paragraph 0019).**

7. As per **claims 3, 26, 86, and 92**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein a said group of PSDs comprises a SATA PSD **(see paragraph 0019).**

8. As per **claims 4, 30, 87, and 93**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein a said group PSDs comprises a PATA PSD and a serial-to-parallel converter **(data interface 144 of fig. 6)** is provided between said device-side IO device interconnect controller and said PATA PSD **(see paragraph 0030).**

9. As per **claims 6 and 32**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein one of said PSDs can be detached from said storage virtualization controller when said storage virtualization controller is on-line **(see paragraph 0019, which discloses "Disc drive 106 can preferably be removed without disturbing the operation of subsystem 100")**.

10. As per **claims 7 and 33**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein a new PSD can be attached to said storage virtualization controller when said storage virtualization controller is on-line **(see paragraph 0030).**

11. As per **claims 10 and 24**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Meehan discloses wherein a said host-side IO device interconnect port and a said device-side IO device interconnect port are provided in the same IO device interconnect controller **(see para. 0029 and fig. 6).**

12. As per **claims 12 and 27**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said storage virtualization controller comprises a plurality of host-side IO device interconnect ports each for coupling to a host-side IO device interconnect **(see fig. 6 and paragraph 0026).**

13. As per **claims 13 and 29**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein said storage virtualization controller is configured to present redundantly a logical media unit on at least two of said plurality of host-side IO device interconnect ports **(see paragraph 0019).**

14. As per **claims 14 and 35**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein

at least one said host-side IO device interconnect port is Fibre Channel supporting point-to-point connectivity in target mode **(see paragraph 0030 and fig. 6)**.

15. As per **claims 15 and 36**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting private loop connectivity in target mode **(see paragraph 0030 and fig. 6)**.

16. As per **claims 16 and 37**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Fibre Channel supporting public loop connectivity in target mode **(see paragraph 0032 and fig. 6)**.

17. As per **claims 20 and 41**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1" **[See rejection to claim 1 above]** Bicknell discloses wherein at least one said host-side IO device interconnect port is Serial ATA operating in target mode **(see paragraph 0019).**

18. As per **claims 34 and 101-103**, the combination of Bicknell, Meehan, and Rinaldis discloses "The virtualization subsystem of claim 21" **[See rejection to claim 21 above]** Bicknell discloses wherein said group of PSDs include a first set of PSDs and a second set of PSDs, said first set of PSDs and said second set of PSDs are not received in a same enclosure **(see figures 3**

and 6), and said storage virtualization controller further comprises at least one multiple-device device-side expansion port **(Midplane Card ports 209 of fig. 6)** for coupling to said second set of said PSDs (**see fig. 6)**.

19. As per **claims 42 and 80**, the combination of Bicknell, Meehan, and Rinaldis discloses "The virtualization subsystem of claim 21" **[See rejection to claim 21 above]** Bicknell discloses comprising an enclosure management services mechanism **[(MUX 208 of fig. 8), in regards to an "enclosure management service", the applicant discloses "*In this embodiment, an enclosure management service (EMS) circuitry 360 is attached to the CPC 240 for managing and monitoring at least one of the following devices belonging to the storage virtualization subsystem 20: power supplies, fans, temperature sensors, voltages, uninterruptible power supplies, batteries, LEDs, audible alarms, PSD canister locks, door locks*". Similarly, Bicknell discloses "The multiplexing electronics selectively opens and closes the first and second data communication paths in response to at least one control signal (such as 218 or 220)"see paragraph 0037. The electronics connection, as discloses, is power supplies]**.

20. As per **claim 43**, the combination of Bicknell, Meehan, and Rinaldis discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism manages and monitors at least one of the following devices belonging to the storage virtualization subsystem: power supplies, fans, temperature sensors, voltages, uninterruptible power supplies, batteries, LEDs, audible alarms, PSD canister locks, door locks **(see paragraph 0031).**

21. As per **claim 44**, the combination of Bicknell, Meehan, and Rinaldis discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support direct-connect EMS configuration **(see fig. 8)**.

22. As per **claim 45**, the combination of Bicknell, Meehan, and Rinaldis discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support device-forwarded EMS configuration **(see fig. 8)**.

23. As per **claims 46, 81, 82, and 83**, the combination of Bicknell, Meehan, and Rinaldis discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said enclosure management services mechanism is configured to support direct-connect EMS configuration and device-forwarded EMS configuration **(see fig. 8)**.

24. As per **claim 50**, the combination of Bicknell, Meehan, and Rinaldis discloses "The virtualization subsystem of claim 42" **[See rejection to claim 42 above]** Bicknell discloses wherein said EMS mechanism further comprises status-monitoring circuitry to communicate with said storage virtualization controller **(see paragraph 0031).**

25. As per **claims 97-100**, the combination of Bicknell, Meehan, and Rinaldis discloses "The storage computer system of claim 1" **[See rejection to claim 42 above]** Bicknell discloses wherein said group of PSDs are received in a plurality of enclosures **(see figures 3 and 6)**.

26. **Claims 11 and 25,** are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Rinaldis et al. (US pat. 7,107,343) as applied to claim 1 above, and further in view of Otterness et al. (US pub. 2002/0152355).

27. As per **claims 11 and 25,** the combination of Bicknell, Meehan, and Rinaldis discloses "The storage virtualization computer system of claim 1," **[See rejection to claim 1 above]**, but fails to disclose expressly wherein said at least one IO device interconnect controller comprises a plurality of IO device interconnect controller; wherein said host-side I0 device interconnect port and said device-side I0 device interconnect port are provided in different said IO device interconnect controllers.

Otterness discloses "wherein said at least one IO device interconnect controller comprises a plurality of IO device interconnect controller; wherein said host-side I0 device interconnect port and said device-side I0 device interconnect port are provided in different said IO device interconnect controllers" **(see fig. 4, which discloses a controller such as a RAID controller 199 having a processor 216 such as the 'central processing circuit' as claimed. Fig. 4 also discloses multiple processor/memory controllers 204 and 206 connected to the processor**

216. Multiple processor/memory controllers 204 and 206 are shown to have their own device port and host port. See para. 0048 for more detail).

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Rinaldis et al. (US pat. 7,107,343), and Otterness et al. (US pub. 2002/0152355) are analogous art because they are from the same field of endeavor of redundant array of independent disks (RAID) architectures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a low cost system for providing improved RAID 1 performance as described Rinaldis, and device interconnection topologies, and methods for communicating data or other information between such devices; more particularly to inter- and intra-device connection and communication topologies and methods for such communication; and most particularly to RAID storage system controllers that increase available storage device interconnect channel capacity by routing controller-to-controller messages to a communication channel separate from the communication channel normally used to communicate the RAID data as taught by Otterness.

The motivation for doing so would have been because Otterness teaches that" **Embodiments of the NorthBay.TM. provides support services for a RAID controller. Among other things, the NorthBay ASIC implements a fast special-purpose-processor that computes the parity values used in the RAID system. The data for which the NorthBay**

ASIC is to handle memory operations and compute parity is specified by the RAID controller's CPU in response to host disk transactions" (see paragraph 0018).

Therefore, it would have been obvious to combine Otterness et al. (US pub. 2002/0152355) and Meehan et al. (US pub. 2004/0177218) with Bicknell et al. (US pub. 2003/0193776) and Rinaldis et al. (US pat. 7,107,343) for the benefit of creating the storage virtualization computer system to obtain the invention as specified in claims 11 and 25.

28. **Claims 17, 19, 38, 40, 47, 48, 84, and 85**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) and Rinaldis et al. (US pat. 7,107,343) as applied to claim 1 above, and further in view of Rabinovitz et al. (US pat. 6,483,107).

29. As per **claims 17, 19, 38, and 40**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1," **[See rejection to claim 23 above]**, including at least one said host-side IO device interconnect port is parallel/serial operating in target mode **(see paragraph 0030)**, but fails to disclose expressly a SCSI.

Rabinovitz discloses a SCSI in a storage virtualization subsystem **(col. 16, line 49).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Rinaldis et al. (US pat. 7,107,343), and Rabinovitz et al. (US pat. 6,483,107) are analogous art because they are from the same field of endeavor of peripheral storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its

Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a low cost system for providing improved RAID 1 performance as described Rinaldis, and a canister and a casing of a computer peripheral enclosure as taught by Rabinovitz.

The motivation for doing so would have been because Rabinovitz teaches that a SCSI allows more connecting storage devices **(see col. 16, lines 43-54).**

Therefore, it would have been obvious to combine Rabinovitz et al. (US pat. 6,483,107) with Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) and Rinaldis et al. (US pat. 7,107,343) for the benefit of creating the storage virtualization subsystem to obtain the invention as specified in claims 17 and 38.

30. As per **claims 47 and 84**, the combination of Bicknell, Meehan, and Rinaldis "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]**, including the enclosure management services mechanism **(MUX 208 of fig. 8)**, but fails to disclose expressly wherein said enclosure management services mechanism is configured to support SES enclosure management services protocol.

Rabinovitz discloses a SES in a storage virtualization subsystem **(col. 17, line 23).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Rinaldis et al. (US pat. 7,107,343), and Rabinovitz et al. (US pat. 6,483,107) are analogous art because they are from the same field of endeavor of peripheral storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its

Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a low cost system for providing improved RAID 1 performance as described Rinaldis, and a canister and a casing of a computer peripheral enclosure as taught by Rabinovitz.

The motivation for doing so would have been because Rabinovitz teaches that a SES allow a user to monitor the enclosure from a remote location **(see col. 17, lines 29-31).**

Therefore, it would have been obvious to combine Rabinovitz et al. (US pat. 6,483,107) with Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) and Rinaldis et al. (US pat. 7,107,343) for the benefit of creating the storage virtualization subsystem to obtain the invention as specified in claims 47 and 84.

31. As per **claims 48 and 85**, the combination of Bicknell, Meehan, Rinaldis, and Rabinovitz discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell discloses the enclosure management services mechanism, and Rabinivitz further discloses the SAF-TE, **(see col. 17, line 29).**

32. **Claims 18, 39, 49, 51, 52, and 53**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218) Rinaldis et al. (US pat. 7,107,343) and as applied to claim 1 above, and further in view of Colton (US pub. 2005/0089027).

33. As per **claims 18 and 39**, the combination of Bicknell, Meehan, and Rinaldis discloses "The computer system of claim 1," **[See rejection to claim 1 above]**, including at least one said host-side IO device interconnect port **(see fig. 6)**, but fails to disclose expressly wherein at least one said host-side IO device interconnect port is ethernet supporting the iSCSI protocol operating in target mode.

Colton discloses ethernet supporting the iSCSI protocol operating in target mode **(see fig. 11 and paragraph 1487, which discloses internet SCSI in an Ethernet network).**

Bicknell et al. (US pub. 2003/0193776), Meehan et al. (US pub. 2004/0177218), Rinaldis et al. (US pat. 7,107,343), and Colton (US pub. 2005/0089027) are analogous art because they are from the same field of endeavor of data transfer.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a disc storage subsystem that allows continued access to data stored in its Advanced Technology Architecture (ATA) disc drives in the event of a controller failure as described by Bicknell and a redundant array of independent disks (RAID) architectures, and more specifically, to a multiple level RAID architecture as taught by Meehan, a low cost system for providing improved RAID 1 performance as described Rinaldis, and a system and method for transferring data optically via an intelligent optical switching network as taught by Colton.

The motivation for doing so would have been because Colton teaches that **"The Sun server(s) running Oracle should have a minimum of 2 high-speed SCSI disk drives to ensure adequate performance" (see paragraph 1487).**

Therefore, it would have been obvious to combine Colton (US pub. 2005/0089027) with Bicknell et al. (US pub. 2003/0193776) and Meehan et al. (US pub. 2004/0177218) and Rinaldis

et al. (US pat. 7,107,343) for the benefit of creating the computer system to obtain the invention as specified in claims 18 and 39.

34. As per **claims 49, 51, and 53**, the combination of Bicknell, Meehan, Rinaldis, and Colon discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell discloses the enclosure management services mechanism and a storage virtualization controller **(see fig. 8)**, and Colon further discloses 12C latches, **(see fig. 11).**

35. As per **claim 52**, the combination of Bicknell, Meehan, Rinaldis, and Colon discloses "The storage virtualization subsystem of claim 42," **[See rejection to claim 42 above]** Bicknell discloses the enclosure management services mechanism as a micro-computer **(see fig. 8)**, and Colon further discloses a CPU for running a program, **(see paragraph 0810 and fig. 11).**

IV. RELEVANT ART CITED BY THE EXAMINER

36. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

37. The following reference teaches a storage virtualization computer system.

U.S. PATENT NUMBER

US 6,574,709; 7,107,320; 2002/0133735; 6,467,034

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

38. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

39. Per the instant office action, claims 1-4, 6, 7, 10-22, 24-27, 29, 30, 32-53, 78-87, 90-93, and 97-103 have received a first action on the merits and are subject of a first action non-final.

DIRECTION OF FUTURE CORRESPONDENCES

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

41. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov.

Should you have questions on access to the Private PAIR system, contact the

Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

January 5, 2009

Ernest Unelus
Patent Examiner
Art Unit 2181

/E. U./

Examiner, Art Unit 2181

/Niketa I. Patel/

Primary Examiner, Art Unit 2181